Patent
Attorney Docket No: RENA-05U1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Franck Delahaye	Examiner: Maki Angadi
Application Number: 10/599,208	Art Unit: 1792
Filed: September 22, 2006	
For: PROCESS FOR THE WET CHEMICAL TREATEMENT OF ONE SIDE OF SILICON WAFERS	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Request for Examiner Interview

Applicant respectfully requests an Examiner Interview to discuss the pending Office Action, primarily with respect to independent claims 1 and 10

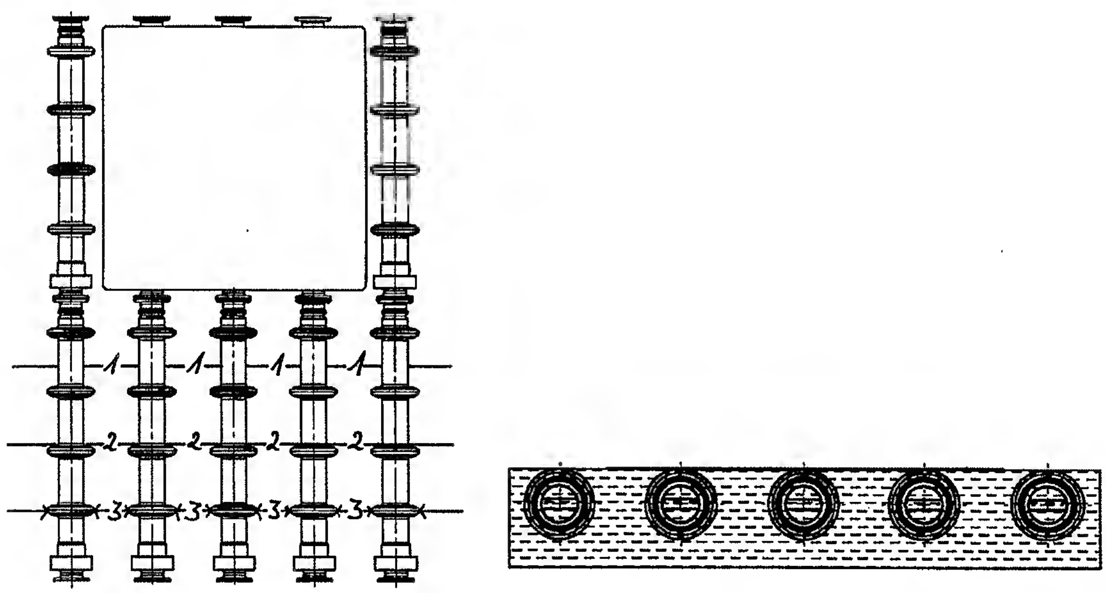
Status of the Claims

Claims 1-27 stand rejected pursuant to a non-final Office Action mailed July 13, 2010. Independent claims 1 and 10 are the subject of the Interview.

Summary of the Claimed Subject Matter

With respect to claim 1, a process for wet-chemical treatment of one side of a silicon wafer using a liquid bath is provided. During the treatment the silicon wafer lays on conveyor means and the entire surface of the underside to be treated is conveyed through or over liquid located in the liquid bath. The conveyor means are positioned within the liquid bath. The top side, which is not to be treated, is always positioned above the liquid. An example of this configuration is depicted as Exhibit A.

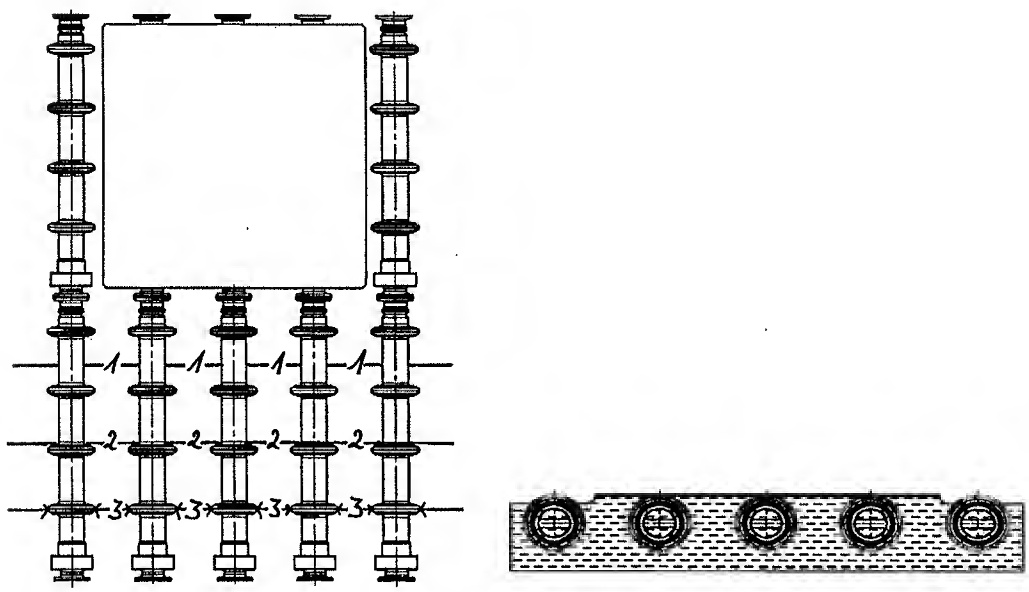
EXHIBIT A



With respect to claim 10, a process for wet-chemical treatment of one side of a silicon wafer using a liquid bath is provided. During the treatment the silicon wafer lays

on conveyor means and is conveyed with the underside to be treated through or over liquid located in the liquid bath. The level of the liquid being contacted by the underside is maintained above the level of the bath surface not being contacted by the underside. The top side, which is not to be treated, is always positioned above the level of the liquid. An example of this configuration is depicted as Exhibit B.

EXHIBIT B



Questions Presented

1. Whether the claims are being examined as the top side which is not to be treated is positioned above the liquid or as a wafer not to be treated is positioned above the liquid.

2. Whether the inclusion of an additional element directed towards the positioning of a meniscus at the wafer would likely traverse the pending rejection over Hiraishi.

Discussion

Question 1:

For clarity, it is respectfully requested to confirm the claims are being examined as selectively treating the underside of each wafer while not treating the top side of each wafer. There appears to be an inconsistency with this conclusion throughout the Office Actions, which may either be a typographical error or require further clarity in the claims. For example, in the pending Office Action, at the end of page 5 crossing onto page 6, it is concluded,

> Hiraishi does not explicitly disclose that the wafer not to be treated is always positioned above the liquid. However, Hiraishi discloses the level of water in the cleaning bath can be controlled. Therefore, one who is skilled in the art should be able to control the water level so that the wafers which are not to be treated are positioned above the liquid.

For completeness, Claims 1 and 10 are directed towards treating the underside of the wafer while not treating the top side of the same wafer. That is, each wafer is to be treated; however, the topside of each wafer is not. Should this require further clarification in the claims, both claims 1 and 10 could be amended to recite:

> further wherein the top side ~~of the wafer~~ which is not to be treated is always positioned above the liquid

Question 2:

In the Office Action, Hiraishi is relied upon as providing a conveyor means for conveying a substrate through a bath. In essence, the Examiner concludes both claims 1 and 10 are obvious over Hiraishi because one of ordinary skill in the art could control the

water level (Office Action at pg. 6) and the level of cleaning liquid and position of wafers is an adjustable parameter, which may be optimized for best results of cleaning or etching (Office Action at pg. 7).

Hirashi's laminate is reproduced below. Referring to Col. 1, ll. 37-46, the photovolataic module includes a glass base substrate (5) joined to a laminate (L), which itself includes a a first electrode layer (3), a semiconductor photovoltaic layer (5) formed from amorphous silicon and a second electrode layer (7).

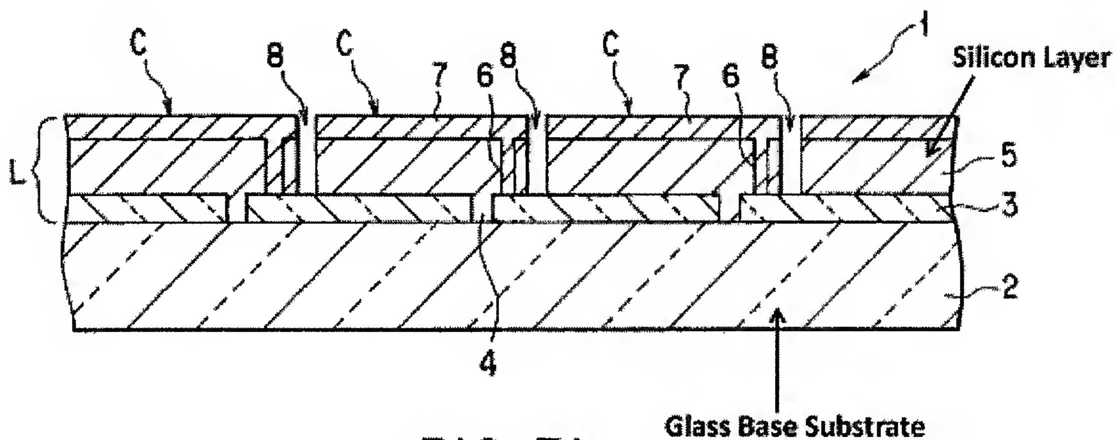


FIG. 7A

Hiraishi confirms that the semiconductor layer (5) or silicon layer is already treated for use in the laminate prior to washing the module. For instance, Col. 1, ll. 62-65 provides,

> The semiconductor photovoltaic layer (5) of amorphous silicon, which includes a p-i-n junction, is deposited on the first electrode layer (3) by plasma CVD. The grooves (6) are formed in the photovoltaic layer (5) by laser scribing, whereby the adjacent photovoltaic cells are connected electrically in series with one another. The grooves (6) also extend straight at right angles to the drawing plane of FIG. 7A. Subsequently, the second electrode layer (7) of metal such as Ag, Al, or Cr is formed to cover the photovoltaic layer 5. The grooves (6) are also packed with this metal. Further, grooves (8) are formed in order to divide the photovoltaic

layer (5) and the second electrode layer (7) into a plurality of regions corresponding to the photovoltaic cells C. The grooves (8), which are also formed by laser scribing, also extend straight at right angles to the drawing plane of FIG. 7A. Preferably, the grooves (8) are deep enough to reach the first electrode layer (3).

The problem solved by Hiraishi relates to technical challenges that occur when laser scribing grooves in laminates. Specifically, debris is left over in the grooves from the laser scribing process, which must be washed away. This is depicted in FIG. 7B reproduced below.

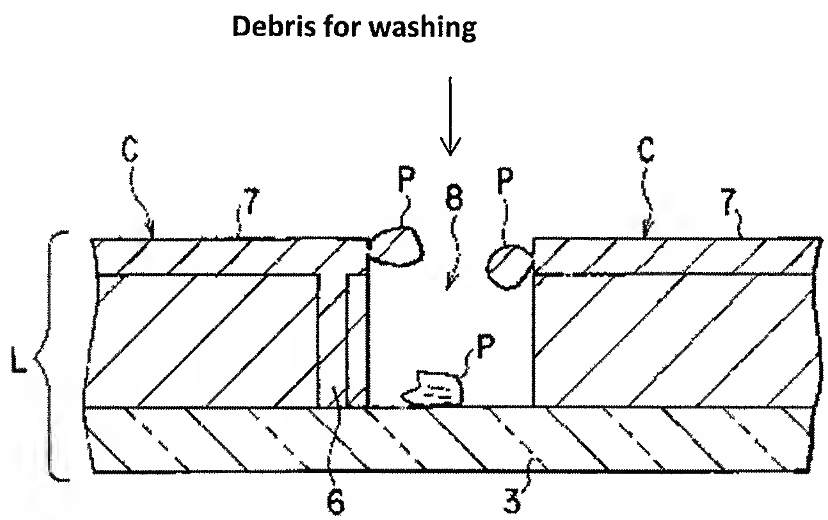


FIG. 7B

While the washing step in Hirashi is directed towards treatment of the entire module, which includes the glass substrate and laminate, the object of the present invention is to treat silicon wafers themselves. Silicon wafers and their treatment are introduced in the present application at page1,

> First of all, a silicon ingot is cut into slices, also known as wafers, using a wire saw. After they have been cut, the wafers are cleaned in order to remove what is

known as a sawing slurry. This is generally followed by a wet-chemical saw damage etch using suitable chemicals, such as in particular lyes, in order to remove the defect-rich layer which results from the cutting process. The wafers are then washed and dried.

The wafers or substrates are generally monocrystalline or polycrystalline silicon wafers which are p-doped with boron. To produce a p n junction required for the solar cell to function, one side of the silicon wafers is n-doped. This n-doping is usually carried out by means of phosphorus doping. In the process, the substrate or silicon surface is modified by the incorporation of phosphorus atoms, the phosphorus source used generally being a gas or a liquid-pasty composition.

When treating silicon wafers, there are technical challenges to overcome. For example, referring to page 2,

One problem with this surface modification is that generally not only the desired surface (top side) but also the opposite surface (underside) and in particular the peripheral edges of the substrate waters are modified or doped by the treatment, which in subsequent use leads to the risk of short circuits, since the edges are electrically conductive.

Now turning to Hirashi's washing step, Hirashi submerges the entire module in a bath and uses ultrasonic vibration to wash the debris from the grooves. This is shown in FIG. 1 reproduced below.

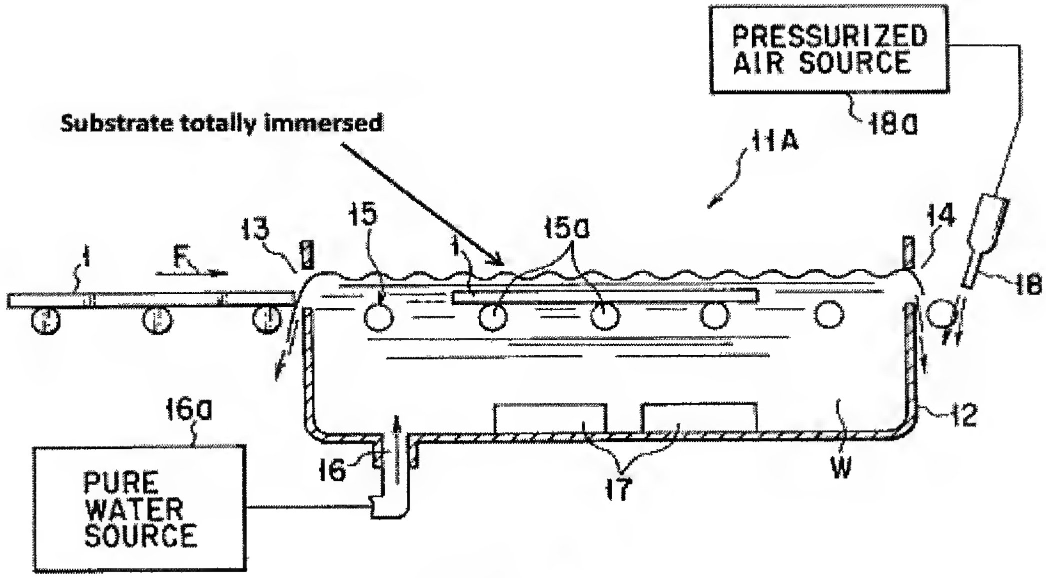


FIG. 1

A total emersion approach was considered in the present application; however, when working with silicon wafers as set forth in the application selective treatment of only one side would require masking as discussed in paragraphs [0010]-[0011],

> By way of example, DE 43 24 647 A1 and US 2001/0029978 A1 describe a multistage etching process in which a substrate is completely immersed in an acid bath. Since it is only the back surface and the edges of the substrate which are being etched here in each case, the front surface of the substrate has to be protected by an acid-resistant photoresist or a mask.
>
> In particular, the etching process described in DE 43 24 647 A1 and US 2001/0029978 A1 is not just time-consuming, since special working steps are required for the application and removal of protective layers, but also requires the use of additional materials. In particular, the application and removal of protective layers entails the risk of the substrates which are to be treated being adversely affected. Should a protective layer applied be defective or damaged, there is a risk of the front surfaces of the substrates being damaged during etching, so that the substrates become unusable

In the Office Action at page 6, the Examiner proposes the skilled artisan could lower the level of the fluid. First, lowering the fluid below the topside would not be consistent with Hiraishi's approach since the scribed grooves and debris are positioned on the topside, and Hiraishi has no need for selective treatment of a single side of a wafer since the silicon layer is applied using sputtering or chemical vapor deposition (CVD) and sandwiched between additional layers. Second the present invention noted a characteristic of silicon wafers cut from ingots that significantly differs from the characteristics of Hiraishi's module. Specifically, silicon wafers tend to float in a bath while Hiraishi's module sinks.

Initially it was expected that any attempt at conveying a silicon wafer along the bath level would cause the silicon wafer to float away due in part to the high surface area to low weight ratio of the silicon wafer as well as adhesion and cohesive forces and the surface tension of liquids. In other words, once a liquid is about the level of a conveyor means or above, it is expected that a wafer will lose contact with the conveyor means and float away from its desired path. Again, this is in contrast to a module that includes a glass substrate base and layered laminate in Hiraishi, which tends to sink in liquids. That is, silicon wafers tend to float when placed in solution; whereas Hirashi's module sinks.

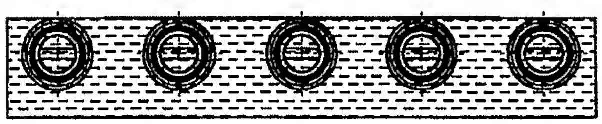
In this regard, it was surprising to learn that the wafer during treatment can be conveyed through or over the liquid in a controlled and targeted manner without floating apart from a predetermined path.

With regard to a first solution, referred to as active or direct wetting, it was found that a meniscus could be formed around the edges and the interplay between surface tension and gravity could overcome the tendency to float away from its desired path. This is summarized at page 10, ll. 19-32,

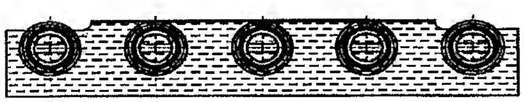
> In the context of the active wetting as defined above, the individual conveyor rolls are preferably arranged in such a manner in a liquid bath that in each case the

upper edge of the rolls is located approximately at the level of the bath surface, i.e. of the upper edge of the liquid, so that the underside of the substrate is wetted through direct contact with the bath surface. In this case, a meniscus may form at the substrate edges. The interplay of gravity and surface tension then draws the substrate downward and ensures that it remains in contact with the rolls without floating. This allows controlled and defined conveying of the substrates using the roll conveyor system.

This active or direct wetting approach is depicted below (Exhibit A):



The second approach is referred to as passive wetting or indirect wetting is the focus of claim 10, where the silicon wafer is conveyed over the surrounding bath. In this case, a meniscus can form at the edge but also between the underside of the wafer and the bath as shown below:



Thus, a further amendment could be considered to clarify the presence of the meniscus discussed above, such as "further wherein a meniscus is positioned at edges of the wafer" with respect to claim 1 and "further wherein a mensius is positioned at edges and between the underside of the wafer and liquid within the liquid bath" with respect to claim 10.

Claims with Proposed Elements

1. (Proposed Amendment) A process for wet-chemical treatment of one side of a silicon wafer using a liquid bath, during which treatment the silicon wafer lays on conveyor means and the entire surface of the underside to be treated is conveyed through or over liquid located in the liquid bath, wherein the conveyor means are positioned within the liquid bath, further wherein the top side ~~of the wafer~~ which is not to be treated is always positioned above the liquid, further wherein a meniscus is positioned at edges of the wafer.

10. (Proposed Amendment) A process for wet-chemical treatment of one side of a silicon wafer using a liquid bath, during which treatment the wafer lays on conveyor means and is conveyed with the underside to be treated through or over liquid located in the liquid bath, wherein the level of the liquid being contacted by the underside is maintained above the level of the bath surface not being contacted by the underside, further wherein the top side ~~of the wafer~~ which is not to be treated is always positioned above the level of the liquid, further wherein a mensius is positioned at edges and between the underside of the wafer and liquid within the liquid bath.

Please contact Attorney of Record, Raymond Wagenknecht at 858-587-2510 x 201 to discuss these questions.

Sincerely,

12/6/2010

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